Patent Claims

1. An electronic component (1) having a multilayered rewiring plate (2), which carries a circuit chip (3), in particular a magnetic memory chip (4), and connects contact areas (5) of the chip to external contacts (7) of the electronic component (1) via rewiring lines (6), the rewiring plate (2) having at least one patterned, magnetic shielding layer (8) made of an amorphous metal or an amorphous metal alloy.

2. The electronic component according to claim 1, characterized in that
the circuit chip (3) has magnetic memory cells.

3. The electronic component according to claim 1, characterized in that
the circuit chip (3) is a logic chip (14).

4. The electronic component according to one of the preceding claims,
characterized in that
the shielding layer (8) is a patterned shielding film (9) having a thickness of between 20 and 75 micrometers.

5. The electronic component according to one of the preceding claims,
characterized in that
the shielding layer (8) has a plurality of stacked shielding films (9) laminated one on top of the other.

6. The electronic component according to one of the preceding claims,
characterized in that
the amorphous metal comprises a cobalt or cobalt alloy.

7. The electronic component according to one of the

preceding claims,
characterized in that
the amorphous metal comprises a boron/iron alloy.

8. The electronic component according to one of the preceding claims,
characterized in that
the amorphous metal has a saturation induction of between 0.5 and 1 tesla.

9. The electronic component according to one of the preceding claims,
characterized in that
the amorphous metal has a saturation magnetostriction of less than 0.2×10^{-6}.

10. The electronic component according to one of the preceding claims,
characterized in that
the amorphous metal has a Curie point of between 200°C and 500°C.

11. The electronic component according to one of the preceding claims,
characterized in that
the patterned shielding layer (8) is arranged on the outer side (10) of the rewiring plate (2), which is opposite to the circuit chip (3), the shielding film (9) having at least openings (11) for external contacts (7) arranged in a predetermined pitch annularly or in a matrix.

12. The electronic component according to one of the preceding claims,
characterized in that
the patterned shielding layer (8) of the rewiring plate (2) of a memory chip (12) has at least one bonding channel opening.

13. The electronic component according to one of the preceding claims,
characterized in that
the patterned shielding layer (8) is arranged on the chip side (15) of the rewiring plate (2) and has at least openings (11) for bonding contact areas (16).

14. The electronic component according to one of the preceding claims,
characterized in that
the circuit chip (3) has a shielding film (9) on its rear side (17).

15. The electronic component according to one of the preceding claims,
characterized in that
the circuit chip (3) has a patterned shielding film (9) on its active front side (18), in which shielding film at least openings (11) for the contact areas (5) of the circuit chips (3) are provided.

16. The electronic component according to one of the preceding claims,
characterized in that
the shielding layer (8) on the rewiring plate (2) has at least a shielding factor of between 50 and 100.

17. A method for producing an electronic component (1) having a multilayered rewiring plate (2), which carries at least one circuit chip (3) and connects contact areas (5) of the circuit chip to external contacts (7) of the electronic component (1) via rewiring lines (6), the rewiring plate (2) having at least one patterned, magnetic shielding layer (8) made of an amorphous metal or an amorphous metal alloy, the method having the following method steps:

- patterning of a shielding film (8) made of amorphous metal or an amorphous metal alloy for a panel with a plurality of component positions,
- lamination of the patterned shielding film (8) onto the rewiring plate (2) of the panel,
- application and electrical connection of circuit chips (23) in the component positions of the rewiring plate (2) of the panel,
- application of a plastic housing composition (19) to the panel embedding the circuit chips (3) and the electrical connections (20),
- application of external contacts (7) in the component positions of the panel,
- singulation of the component positions of the panel to form individual electronic components (1).

18. The method according to claim 17,
characterized in that
the patterning of the shielding films (9) is effected by means of stamping predetermined patterns of openings (11).

19. The method according to claim 17,
characterized in that
the patterning of the shielding films (9) is effected by means of laser removal.

20. The method according to claim 17,
characterized in that
the patterning of the shielding films (9) is effected by means of etching methods through an etching mask.

21. The method according to one of claims 17 to 20,
characterized in that
prior to the application of the circuit chips (3) to the chip side (15) of the rewiring plate (2), which carries the circuit chips (3), the patterned shielding film (9) is laminated on leaving the areas provided for

the bonding connections (21) free.

22. The method according to one of claims 17 to 20, characterized in that
the patterned shielding film (9) is laminated onto the outer side (10) of the rewiring plate (2), which carries the external contacts (7), with the areas provided for the external contacts (7) being left free.

23. The method according to one of claims 17 to 22, characterized in that
in the component positions of the panel, circuit chips (3) with magnetic memory cells are applied to the rewiring plate (2).

24. The method according to one of claims 17 to 23, characterized in that
in the component positions of the panel, circuit chips (3) with logic circuits are applied to the rewiring plate (2).

25. The method according to one of claims 17 to 24, characterized in that
a plurality of patterned shielding films (9) are laminated one on top of the other.

26. The method according to one of claims 17 to 25, characterized in that
prior to the application of the circuit chips (3) to the rewiring plate (2), shielding films (9) are applied on the rear sides (17) of the circuit chips (3).

27. The method according to one of claims 17 to 26, characterized in that
prior to the application of the circuit chips (3) to the rewiring plate (2), patterned shielding films (9) are applied on the active front side (18) of the circuit chips (3) with the contact areas (5) of the

circuit chips (3) being left free.